IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPELLANT:	Dee Gardiner
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FOR:	METHOD FOR REDUCING TRANSPORT DELAY IN AN IMAGE GENERATOR
ART UNIT:	2628
EXAMINER:	Roberta D. Prendergast
DOCKET NO:	2469-T9180

CERTIFICATE OF DEPOSIT

DATE OF DEPOSIT: December 3, 2007

I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being electronically deposited using EFS Web with the United States Patent Office on the date indicated above.

/Steve M. Perry/

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APPELLANTS' APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Mail Stop Appeal Brief – Patents

Sir:

Appellants submit this Amended Appeal Brief in connection with their appeal from the final rejection of the Patent Office, mailed February 27, 2007, in the above-identified application. A Notice of Appeal was filed on June 26, 2007. The amended brief includes all of the formal amendments suggested in the Examiner's Answer. Additionally, to comply with 37 CFR 41.37(c) the status identifiers for the claims in Sections V and VIII have been removed.

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I. REAL PARTY IN INTEREST

The real party in interest of this application is Rockwell Collins, Inc., 400 Collins Rd N.E., Cedar Rapids, IA 52498.

II. RELATED APPEALS AND INTERFERENCES

Appellants and Appellants' legal representatives know of no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 10-14, 24, 26-29, 32 and 34-35 remain pending. Claims 1-9, 15-23, 25, 30, 31, 33, and 36-38 have been previously canceled. Claims 10-14, 24, 26-29, 32 and 34-35 stand rejected. The claims on appeal in this application are 10-14, 24, 26-29, 32 and 34-35.

IV. STATUS OF AMENDMENTS

Claims 10, 24, 32, 34 and 35 were amended after the Office Action mailed February 27, 2007 and were entered to place the application in a better condition for appeal. Claims 25, 30-31, 33 and 36-38 were cancelled without prejudice. The Examiner has withdrawn the 35 USC § 112, second paragraph rejection of claims 25, 30, 31, 33-35 and 37. Claims 10-14, 24, 26-29, 32, 34 and 35 stand rejected under 35 USC 102(e) and 103(a) as written in the Office Action mailed February 27, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

10. A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins 152 (page 10, lines 13-15);

(b) storing primitives 154 in each screen bin 152 the primitives touch (page 10, lines 15-17);

(c) rendering 144 the screen bins 152 by row from top to bottom, into the single pixel frame buffer (page 10, lines 3-5);

(d) displaying 142 at least one row of screen bins 152 rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins 152 takes place after a selected portion of the screen bins for a current field have been rendered. (page 11, lines 5-11).

24. A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins 152 (page 10, lines 13-15);

(b) storing primitives 154 in each screen bin 152 containing a portion of the primitive (page 10, lines 15-21, FIG. 6);

(c) rendering 144 the screen bins 152, by row from top to bottom, into the single pixel frame buffer (page 11, lines 3-5); and

(d) displaying 142 at least one rendered screen bin 152 when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed (page 14, lines 20-21).

32. An image generator with a single pixel frame buffer enabled for simultaneous rendering and display, comprising:

(a) a geometry buffer divided into a plurality of screen bins 152 (page 10, lines 13-15);

(b) a plurality of primitives 154, stored in all of the screen bins 152 that touch a screen region defined by the screen bin 152 (page 10, lines 15-21);

(c) a rendering engine 144, configured to render the primitives in the screen bins 152 into the single pixel frame buffer by row and from top to bottom (page 11, lines 3-14);

(d) a display processor 142, configured to display at least one rendered screen bin 152 on a display screen 150 before the rendering engine 144 has completed rendering all the screen bins 152 (page 8, lines 11-12; page 11, lines 3-7); and

(e) wherein the display processor 142 begins to display the screen bins 152 rendered when the rendering 144 of the screen bins 152 is at least ½ complete (page 14, lines 20-21).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review are:

a. whether independent claim 10 and dependent claims 11 and 13 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,864,342 (hereinafter "Kajiya");

b. whether dependent claims 12 and 14 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Kajiya in view of U.S. Patent No. 6,853,381 (hereinafter "Grigor").

c. whether independent claims 24 and 32 and dependent claims 26-29, 34 and 35 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Kajiya in view of U.S. Patent No. 6,316,974 (hereinafter "Taraci");

VII. ARGUMENT

A. Prosecution History

The present application was filed as an original utility application on October 23, 2000 under the title METHOD FOR REDUCING TRANSPORT DELAY IN AN IMAGE GENERATOR. Twenty three claims were presented. The application was assigned Serial No. 09/694,411.

A Notice of Allowance was mailed on May 5th, 2003. Claims 1-23 were allowed. The Primary Examiner, Cliff Vo, stated that reasons for allowance were that "none of the cited prior art shows an arrangement of the steps/means for dividing, storing, rendering and displaying in order to form a method and system for enabling a single frame buffer for simultaneous rendering and display in a computer image generator as now claimed." The issue fee was paid on July 22, 2003.

A first Office Action mailed on May 11, 2005 was received from Examiner Vo. He advised that the Notice of Allowance was vacated and that the allowability of claims 1, 3, 4, 15, 17-20 and 22-23 was withdrawn in view of the newly discovered reference to Kajiya et al, U.S. Patent No. 5,864,342. Claims 10-14 were allowed. Claims 2, 5-9, 16 and 21 were objected to as being dependent upon a rejected base claim. Claims 1, 3, 4, 15, 17-20, 22 and 23 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kajiya.

Appellants submitted a response to the Patent Office on August 11, 2005. In this response, Appellants argued that Kajiya teaches a method for using a double frame buffer to reduce the amount of depth memory used (Kajiya, Col. 10, lines 47-60), while the present invention includes the limitation of "**a single pixel frame buffer** for simultaneous rendering and display in a computer image generator."

A second Office Action mailed on February 10, 2006 was received from Examiner Vo. The same claims were allowed, objected to, and rejected as in the previous Office Action. The Office Action was made final. The Examiner asserted that Kajiya teaches a method and system for rendering graphical objects to image chunks utilizing a single pixel frame buffer, citing Kajiya, Col, 6, lines 15-19 for support.

Appellants submitted a response to the Patent Office on April 21, 2006. In this response Appellant amended the claims such that claims 2, 16, and 21 were cancelled and rewritten in independent form including all of the limitations of the base claims 1, 15 and 20 respectively. Claims 10-14 had been allowed. Therefore, Applicant submitted that claims 1, 3-15, 17-20, and 22-23 were placed in a condition for allowance.

An advisory action was mailed on May 25, 2006 from Examiner Roberta Prendergast. Rewriting the dependent claims 2, 16 and 21 in independent form including all of the limitations of the base claims 1, 15 and 20 respectively was deemed to require additional searching. Therefore, the amendment was not entered.

Appellants submitted an after final response to the Patent Office on July 7, 2006. All claims were cancelled without prejudice except for claims 10-14 to put the claims in a condition for allowance.

A fourth Office Action mailed August 28th, 2006 was received from Examiner Prendergast. Claims 10, 11, and 13 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kajiya. The Examiner asserted that Kajiya teaches a method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, stating that the single rasterization buffer cited in Kajiya at Column 6, lines 15-29 is understood to be a single pixel frame buffer. Claim 12 was

rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya in view of Grigor et al., U.S. patent No. 6,853,381. The Examiner stated that Kajiya does not specifically teach the step of reducing the transport delay and allowing the display step to overlap a rendering envelope. The Examiner asserted that Grigor teaches this limitation, citing the Abstract, FIGs 1 and 8, column 3, lines 13-33 and column 8, lines 32-67. The Examiner stated that these references disclose that individual display lines comprising a plurality of pixels are rendered and stored in the frame buffer in a memory location only if the location has been previously accessed for display.

Appellants submitted a response to the Patent Office on November 28, 2006. After attempting to put the claims in a condition for allowance four separate times, which eventually resulted in cancelling all claims except 10-14, Appellants reinstated claims 1-9 and 15-23 as claims 24-38. A detailed discussion distinguishing the present invention from Kajiya was included in the response. Regarding the use of a single pixel frame buffer, Appellant argued that Kajiya does not disclose this limitation. The only reference made in Kajiya to a single buffer (Kajiya, Col. 6, lines 15-19), which has been repeatedly relied upon by the Examiners in the continued rejections, is a "single rasterization buffer" cited in the summary of the patent. In the next paragraph of Kajiya, it is explained that the single rasterization buffer is a double buffer. Kajiya does not teach or suggest the idea of using a single pixel frame buffer, but describes on several occasions the use of a double-buffering system, as is standard in the art. Therefore, Appellant argued that the correct interpretation of the cited reference in the patent summary (Col. 6, lines 15-19) is that the system in Kajiya can use a single rasterization buffer that is double buffered.

A fifth Office Action mailed February 27, 2007 was received from Examiner Prendergast. Claims 10-14 and 24-38 were rejected. Claims 25, 30, 31, 33 and 37

were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 10, 11, and 13 were rejected under 35 U.S.C. 102(e) as being anticipated by Kajiya. The Examiner again argued that Kajiya teaches a method for enabling a single pixel frame buffer, citing column 6, lines 15-29 and asserting that the single rasterization buffer is understood to be a single pixel frame buffer. Claim 12 was again rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya in view of Grigor. Claims 24-38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya in view of Taraci et al., U.S. Patent No. 6,316,974.

Appellants submitted a response to the Patent Office on June 26, 2007. Claims 25, 30, 31, 33 and 37, that had been rejected under 35 U.S.C. § 112, were cancelled without prejudice. Claims 10, 32, 34 and 35 were amended to correct for antecedent basis issues. The amendments were made to put the claims in a better form for consideration on appeal under 37 C.F.R. § 1.116. After realizing that little to no progress had been made in the prosecution of the present invention over five separate Office Actions and responses, it was determined that it was in the Appellants' best interest to file an appeal. The Notice of Appeal was filed concurrently with the response on June 26, 2007.

An Advisory Action mailed July 5, 2007 was received from Examiner Prendergast. The Advisory Action stated that the 35 U.S.C. § 112 rejection made in the previous Office Action had been withdrawn and the amendments were entered. The rejections 10, 11 and 13 and 12, 14, 24, 26-29, 32, 34 and 35 under 35 U.S.C. 102(e) and 103(a), respectively, remained.

B. Appellants' invention

Reducing Lag Time

Appellants' invention is directed to a method for reducing transport delay in an image generator. The present invention is useful in real-time image generation of computer generated images used in fields such as simulators used to instruct and train operators such as pilots and drivers. Transport delay is the time between when a stimulus occurs, such as a pilot moving a control stick in a simulator, until the last pixel of the generated image is drawn on a display. In other words, it is the lag that occurs between a user instructing a computer generated image to change and when the image has completed updating.

In the real world, high performance vehicles such as cars and jet planes respond rapidly to a user's commands. In the virtual world of simulators, it takes a set amount of time for a computer to regenerate an updated image based on the user's input. For example, when a fighter pilot directs his plane in a new direction the computer must re-generate a new image based on the new course the plane. If the lag time, or transport delay is not sufficiently short, the delay between the user's action and the reaction displayed on the screen can cause motion sickness. This phenomenon is commonly referred to as simulator sickness.

A standard graphics pipeline architecture used in computer graphics generation for real-time simulation is illustrated in FIG. 4 of the application and reproduced below.

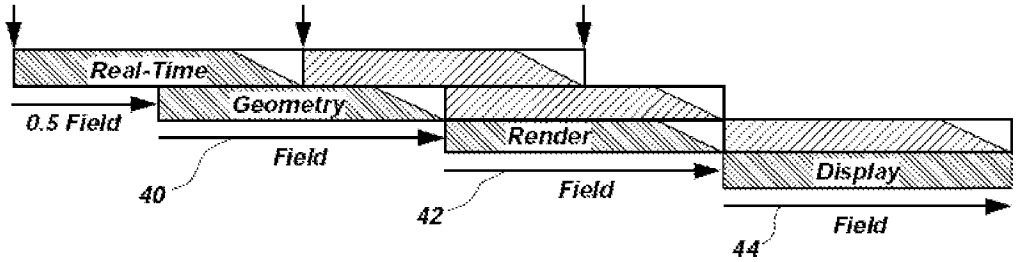


Fig. 4
(PRIOR ART)

The dark shaded boxes represent the flow of one field of data through the graphics pipeline. Each box has a length corresponding to an amount of time it takes to display an image on a screen. At a standard refresh rate of 60 Hertz, a new image can be displayed in approximately $1/60^{th}$ of a second, or 16.67 milliseconds (ms).

The Real-Time box illustrates the time it takes for a real-time controller to receive information from a user, such as a change in direction of a simulated vehicle, and compute the matrices and other information needed to display the scene. A typical time is approximately half a field, or 8.33 ms. The real-time calculations are sent to a geometry processing engine 40 that processes the primitives in each scene. A double buffered memory, referred to as the geometry buffer, is typically used by the prior art between the geometry and rendering 42 processes. This provides one full field time for geometry calculations 40 and the next field time for pixel rendering 42. A second double buffered memory is used by the prior art between the rendering process and the display process 44, typically referred to as a pixel frame buffer. Once the new image has been rendered and written into one side of the double buffered pixel frame buffer, the buffer will be ready to toggle, or swap, at the beginning of the next graphics frame, or field time.

Thus, as illustrated in FIG. 4, a typical lag time between a user's action and the refreshing of the computer generated image on the screen is about 3.5 fields, or about 58.33 ms at a 60 Hertz refresh rate.

The present invention provides methods for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator. As illustrated in FIG. 12 of the Application, which has been reproduced below, a single buffered pixel frame buffer can enable a portion of the rendering process 144 and the display process 142 to occur concurrently.

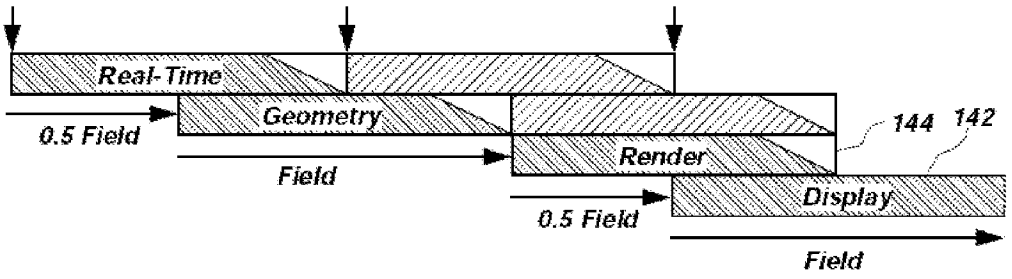


Fig. 12

For example, a portion, such as a single image line, or half of the lines in a computer generated image, can be rendered and stored into the single pixel frame buffer. The display process can then begin retrieving the stored information from the single pixel frame buffer and displaying rendered pixels on the simulator screen. The portion of the image that is rendered and stored in the single buffered pixel frame buffer depends on a difference in time it takes for the rendering process and the display process to occur. If the two processes occur in a relatively similar amount of time, a single line of an image may be stored in the single buffered pixel frame buffer before the display process retrieves the information. If there is more disparity

between the speeds off the two processes, more delay, such as rendering of half the screen, may be needed.

The amount of time that can be saved by using a single pixel frame buffer is significant. At least half of a field time can be shaved off of the total lag time by concurrently running the rendering process 144 and the display process 142 together for at least half a field. Using the previous example, at a display rate of 60 Hertz, the lag time can be reduced from 58.3 ms to 50 ms, a 14% reduction in lag time. If the rendering and displaying processes are closer in time, nearly an entire field of time can be saved, allowing the lag time to be reduced to just over 2.5 fields or 41.67 ms for a 28% reduction in lag time. Thus, the present invention provides a significant improvement in the real-time generation of images by reducing lag time to increase simulator performance and reduce cases of simulator sickness.

Chunking Architecture

In order to render high-quality scenes, many systems store not only the color of each pixel, but compute the color for multiple sub-pixels within each pixel for anti-aliasing. Along with the color values, depth values are computed and stored in order to determine which primitives are in front and which are behind. This sub-pixel frame buffer requires a lot of memory, and more importantly, a lot of memory bandwidth. Memory bandwidth is the speed at which memory can be accessed. Real-time systems typically require rapid access. Thus, high-quality and high-performance systems tend to be very expensive due to the need for large amounts of the fastest types of memory available.

"Chunking" architectures have been used for many years as a way to reduce the cost of memory associated with real-time graphics generation. The Assignee of the present invention has been using chunking architectures since the late 1980's. As

evidence, a portion of a user manual of a system sold by the Assignee entitled "ESIG-3000/2000 System Overview" and published on June 3, 1991, is included in the Section X Evidence Appendix. The user manual discloses a system that includes a Clipper Section (see page 6) in which the display screen is divided up into a uniform grid of 32 x 32 pixel areas called macro spans. These macro spans are equivalent to the 32 x 32 pixel chunks that will be described below in the Kajiya prior art reference. Chunking architectures are used to reduce the amount of memory needed in a computer graphics device since memory is typically one of the more expensive components in the computer graphics device.

In a typical chunking architecture, the amount of memory is reduced by dividing a screen into smaller areas. Rather than store the sub-pixels for the entire screen, the sub-pixels are only stored for one "chunk" of the screen. A chunk is a rectangular block of pixels often about 32x32 pixels in size. The "chunk buffer" is a mini-frame buffer that stores the sub-pixel depth and color values for the pixels within the chunk. After performing the anti-aliasing operations, a single resolved pixel color is then stored in the full screen frame buffer. Thus the chunking architecture removes the need for very large, high bandwidth memory frame buffers and replaces it with a smaller high bandwidth chunk buffer which is much less costly to build.

One disadvantage of this architecture is that the primitives must be sorted into bins associated with each chunk. This bin memory is also double buffered, and therefore adds one more frame of latency to the rendering process. A flow chart illustrating a typical chunking architecture is illustrated in FIG. 5 of the present application and has been reproduced below.

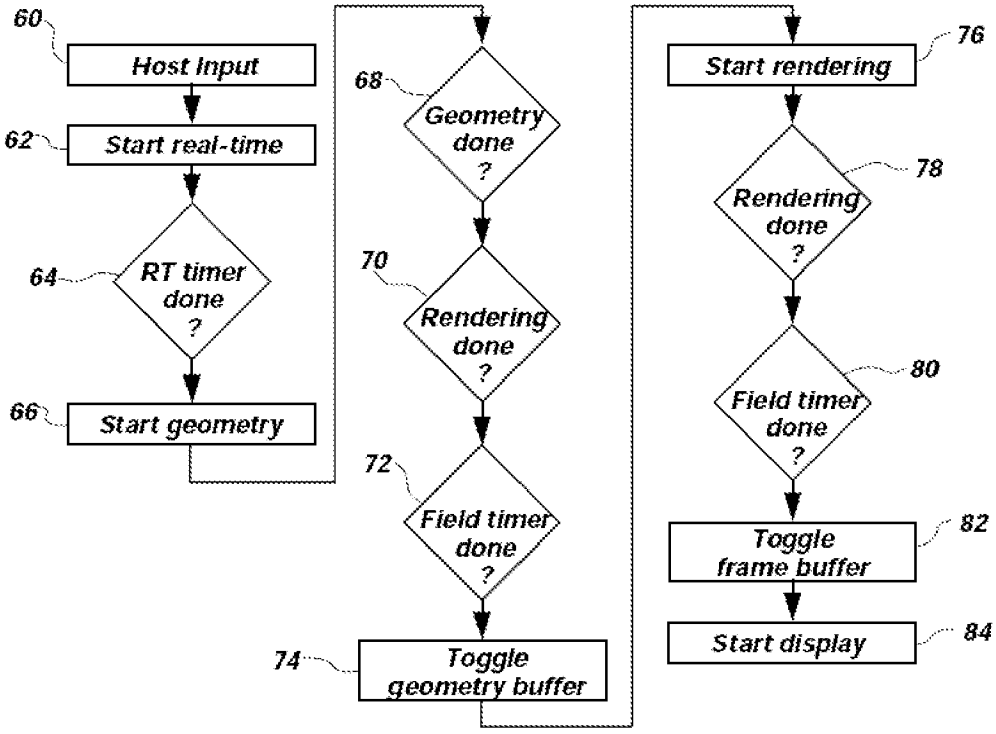


Fig. 5
(PRIOR ART)
"Chunking Architecture"

At the beginning of each new frame, both the frame buffer and the bin memory are toggled. There are now three distinct operating domains; the first is the binning process, second is the rendering operation, and finally the display process. This illustration correlates with FIG. 4 displayed above. As in FIG. 4, the real time process 64 illustrated in FIG. 5 would take approximately half of a frame time, resulting in an overall lag time of approximately 3.5 frames.

Each of the primitives within the scene must be tested against the bins associated with each "chunk" of the screen. The primitives are thereby sorted in to screen related bins. The present invention provides that each primitive that is on screen will be stored in one or more bins. The basic rendering operations are the same as in the

traditional architecture discussed above, but rather than render each primitive to completion, only the portions of the primitives overlapping the current bin are rendered. One bin at a time is rendered, but the bins can be rendered in any order.

Once all of the primitives touching one bin are rendered, the "chunk" buffer can be toggled, the results anti-aliased, and the resolved pixel color can be stored in the full screen frame buffer.

Reduced Lag Time with Chunking Architecture

As previously discussed, the extra frame of delay introduced by the binning process can be problematic in real-time image generation. By selecting a top-to-bottom order of rendering the bins, and by using a single buffer frame buffer, it is possible to remove the extra frame of delay. A flow chart depicting one embodiment of the present invention is illustrated in FIG. 13 and has been reproduced below.

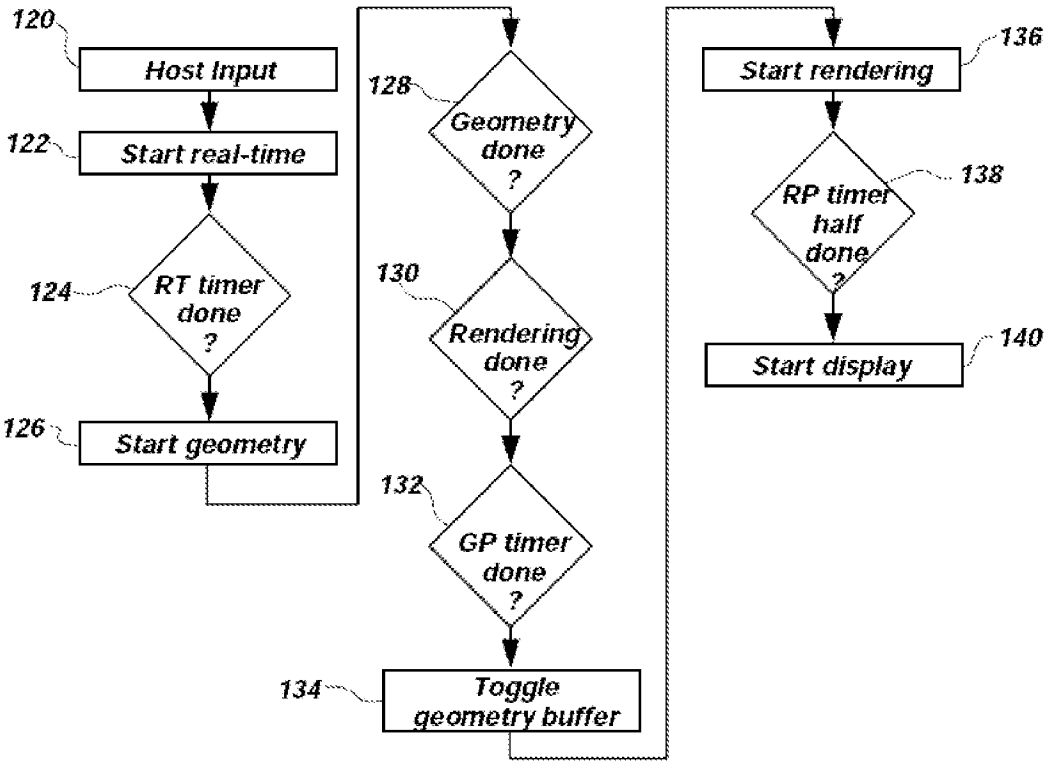


Fig. 13

Reduced Latency Chunking Architecture

As in the previous example, the bin memory is toggled at the beginning of each field. However, in the reduced latency chunking architecture illustrated in FIG. 13 there is not a double buffered frame buffer to toggle. With a standard single buffered frame buffer, primitives are typically updated as they are drawn. With the method disclosed in the present application that distracting artifact is avoided by rendering at least one full row and then displaying that row. The bins are rendered in a top-to-bottom order. The order of bins within a given row is irrelevant, but the top row is completely rendered before the next row begins. Once a complete row has been rendered, that row can then be displayed without waiting for the entire scene to be rendered.

For most display devices, the flow of pixels must be a steady stream without interruption. Thus, care is typically taken to insure that each new row of chunks can be rendered before the previous row has been displayed. Since the rendering complexity is often not uniform on screen, it may be necessary to buffer up multiple chunk rows before starting the display process. FIG. 13 illustrates an embodiment wherein half of the rows are rendered prior to the display process. Rendering the bins for the first half of the rows in a computer generated graphical image provides a larger head start that allows for greater differences in the time it takes to render the bins and place them into the single pixel frame buffer, and the time it takes to display the rendered bins.

A single buffering process requires additional complexity that is not required when a double buffer is used. A double buffer allows an entire display frame to be rendered and stored on one side of the double buffer, then toggled to the other side of the double buffer for displaying. Thus, the double buffer eliminates potential interference between the rendering process and the display process if the two processes occur at different speeds. With a single buffer, if the rendering process and display process occur at different speeds, extra care must be taken to ensure that one process does not encroach on the other.

Since the frame buffer is single buffered in the present invention, if the rendering operations fall too far behind the display process, portions of an old frame will be redisplayed and produce an erroneous picture. Alternatively, if the rendering operations get too far ahead of the display process, the newly rendered data stored in the single buffered frame may overwrite sections that have not been displayed yet. Thus, appropriate measures can be taken to keep the two independent processes from bumping in to each other.

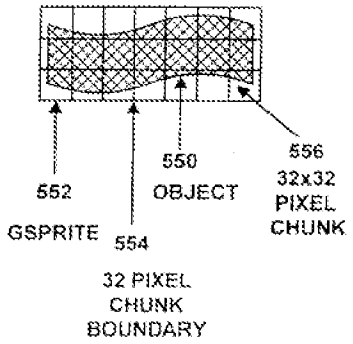
C. The Asserted References

1. The Kajiya Reference

Kajiya discloses a method for reducing the amount of processing required to update a computer generated graphical image by only updating altered portions of an image when a change in view point has occurred by transforming the object geometry of the altered portions using an affine transform based on the change in view point. (See Col. 14, line 43 to Col. 15, line 37).

Kajiya uses a chunking method that involves dividing a scene into non-interpenetrating objects 550 referred to as gsprites 552, as illustrated in FIG. 15B of Kajiya which has been reproduced below. The gsprites are then divided into rectangular chunks 556 such as 32 x 32 pixel regions. (See Col. 10, lines 35-42; Col. 32, lines 30-35).

FIG. 15B



Kajiya discloses a process used to reduce transport delay between a user instructing a computer generated image to change, and when the image has completed updating. The process disclosed in Kajiya takes advantage of the affine transform in combination with the chunking architecture disclosed in Kajiya to warp gsprites that have changed due to a change in viewpoint. (See generally, Col. 56, line 18 to Col.

57, line 34). The process disclosed in Kajiya is significantly different from the claimed invention in the present application.

The process to reduce transport delay disclosed in Kajiya involves using viewpoint data from a subsequent image to affine transform, or warp affected objects or gsprites. (Col. 56, lines 41-51). An affine transformation matrix is computed based on the modeling transform for the current image and the subsequent image. This enables a quick adjustment when rapid changes in viewpoint perspective of a user occur. (Col. 56, lines 52-60).

Kajiya discloses in more detail the actual implementation of the affine transform display method to reduce transport delay. (See generally, Col. 58, line 24 to Col. 62, line 16). Gsprite chunk image data is rendered and affine transforms are calculated for a frame. (Col. 59, lines 62-67). A gsprite engine maps the gsprite image to output device coordinates and transforms the gsprite data. Pixel data is then sent to a double buffered compositing buffer that allows pixel data to be transferred from one buffer while pixel data is being composited in the other buffer. (Col. 60, lines 1-7).

Kajiya discloses another embodiment in which a display device is divided into bands. The term "band" refers to the amount of time (band period) allotted to process a band of pixel data. The time can be derived, in part, from the frame rate and the number of bands in the display device. (Col. 60, lines 54-59). While the gsprite engine fills the compositing buffer for one band, the compositing buffer transfers composited image data for another band to a digital to analog converter. In the next band period, the band that was composited is then displayed. (Col. 60, lines 60-67). The two compositing buffers ping-pong back and forth so that as one scanline region is being displayed, the next is being composited. (Col. 61, lines 5-13).

2. The Grigor Reference

Grigor discloses a write behind controller configured to receive information from a display device controller in order to determine a current location available in a frame buffer for receiving information. Write access to the frame buffer by a rendering engine is prohibited if the access is to an area below a currently available location of the frame buffer. The rendering engine is stalled when the requested address location has not yet displayed its data. Subsequently, the write access to the frame buffer is allowed when the address has been rastered. (See Col. 8, lines 22-60; Abstract).

3. The Taraci Reference

Taraci teaches a method and apparatus for vertically locking input and output video frame rates from digital video sources to eliminate mixing of pixels from different input frames having different resolutions and scan rates into one output frame. This is accomplished using two phase locked loops (PLLs) that are connected in series. (See Col. 13, lines 16-47). The use of two PLLs provides the ability to lock output and input vertical sync pulses by adjusting a reference frequency to the pixel clock generating PLL. Applications include graphics switching, scan conversion, video scaling, line doubling, and line quadrupling. (Col. 18, lines 12-31).

C. Rejections Under 35 U.S.C. § 102(e)

1. Requirements for anticipation

The Examiner has rejected pending claims 10, 11 and 13 under § 102(e) as being anticipated by Kajiya. It should be noted that Kajiya issued as a patent on January 26, 1999, some 21 months prior to the filing of the present application on October 23,

2000. Thus, it appears a rejection under 35 U.S.C. 102(b) would be accurate. Regardless, the analysis of the §102 rejection is the same whether the rejection is based on §102(e) or §102(b). The issue at hand is whether the invention was fully described in the Kajiya patent.

2. The rejection of Claims 10, 11 and 13 as being anticipated by Kajiya

According to MPEP §706.02 (IV), the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. Appellants submit that the Examiner has failed to show that Kajiya teaches every aspect of the claimed invention. The Examiner has repeatedly relied on a reference to the summary in Kajiya, Col. 6, lines 15-29 as evidence that Kajiya teaches the use of a single pixel frame buffer. As Appellants have argued continually, the elements disclosed in Kajiya do not correspond to those of Appellants' invention.

Independent claim 10 of the present application reads as follows:

10. A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins;

(b) storing primitives in each screen bin the primitives touch;

(c) rendering the screen bins by row from top to bottom, into the single pixel frame buffer;

(d) displaying at least one row of screen bins rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins takes place after a selected portion.

As previously discussed, Appellants invention uses a single pixel frame buffer configured for simultaneous render and display of computer graphics image

information in a computer image generator. The single pixel frame buffer enables a reduced transport delay by reducing the number of frames of delay in the computer image generator between a user instructing a computer generated image to change, and when the image has completed updating.

Buffers are typically used to accommodate delay between different processes. Double frame buffers allow a first process to write to a first frame of the buffer. The contents of that frame can then be toggled to the second frame of the double frame buffer, which can be read by a second process. In contrast, if a single frame buffer is used, the same buffer is used for writing by the first process and reading by the second process. Thus, the use of a single frame buffer causes added complexity since it must be ensured that the first process does not overwrite data that has not yet been read by the second process, or that the second process does not read the same data twice that has not been updated by the first process.

In the present invention, a single pixel frame buffer is used between the rendering and displaying processes to reduce the added delay associated with the use of a double frame buffer. The present invention discloses the use of a hardware interlock which can be used to ensure that the rendering process and displaying process do not interfere with each other when using a single buffer between the processes. (See Application, page 14, lines 3-8).

The Examiner has repeatedly cited the summary of Kajiya, Col. 6, lines 15-29 as evidence that Kajiya teaches the use of a single pixel frame buffer. In the Final Office Action mailed February 27, 2007, the Examiner states that the single rasterization buffer recited in this citation is understood to be a single pixel frame buffer." (See Page 4). The entire citation in Kajiya reads:

> The geometry for a chunk can be rendered to a common depth buffer or rasterization buffer. For example, all of the geometry for a first chunk can be rasterized into a single rasterization buffer before geometry for the next chunk is rasterized to the same rasterization buffer. Similarly, pixel data generated while rasterizing primitives for a chunk, including pixel fragments to support high-quality anti-aliasing and translucency computations, can be resolved for a first chunk before the next chunk is resolved. Using a common depth or rasterization buffer saves memory. Moreover, the process of resolving each chunk in this manner provides an effective form of compression because pixel fragments need not be stored before an entire frame of image data is generated.
>
> **The rasterization buffer can be double-buffered** such that the geometry for a first chunk is rasterized to generate pixel data, while the pixel data for another chunk is being resolved. This capability enables sophisticated anti-aliasing and translucency computations to be performed without adding delay in the rendering pipeline. (Col. 6, lines 15-34; emphasis added)

A brief overview of the process disclosed in Kajiya will be helpful in understanding what the rasterization buffer is and how it is used. The graphical image display process disclosed in Kajiya is substantially more complex than the process disclosed in the present application. Kajiya not only renders graphical images, but also performs affine transformations on the rendered images to reduce the amount of computing needed to display the images as the viewpoint changes. The rasterization buffer is part of an image processor 462 for producing rendered image data from geometric primitives, as illustrated in FIG. 4b of Kajiya. Kajiya explains that the rasterization buffer is not a single buffer, but a group of buffers that includes pixel buffers 472 and a fragment buffer 470. The rasterization buffer supports double

buffering of pixel data and single buffering of fragment data. The fragment data occurs due to the gsprite chunking process used in Kajiya. (Col. 61, lines 37-58).

FIGs. 9a-9c of Kajiya illustrate that the rasterization buffer (comprising the fragment buffer(s) 410 and the pixel buffers 408) are part of the Tiler 200. The Tiler 200 is shown in FIG. 4a, located at the beginning of the rendering process. Graphical information is sent to the Tiler 200 to render the images. The rendered data is then sent to the gsprite engine 204 where warping using affine transformations occurs. Information from the gsprite engine 204 is then sent on to post-processing 210 where alpha (opacity) and color buffers are implemented, and finally the digital data is sent to a digital to analog converter (DAC) 212 before being sent to a display device.

In contrast, the single pixel buffer in the present invention is placed between the rendering process 144 and the display process 142, as illustrated in FIG. 12. No warping or affine transformation occurs in the present invention. The single pixel buffer enables a single row of a graphical display to be rendered into the buffer before the display process scans the rendered row. (See specification, page 11, lines 3-14). The transport delay can be reduced using the single pixel frame buffer, which can be accessed by both the rendering and display processes. (Page, lines 10-19).

The single pixel buffer, as used in the present application, is more akin to the compositing buffer disclosed in Kajiya. The compositing buffer is used to collect and hold information ready for display until it is displayed. However, the compositing buffer in Kajiya is a traditional double buffer where transformed chunks are composited together to form an image. (See Kajiya, Col. 60, line 59 to Col. 61, line 13). Kajiya does not take advantage of a single buffer compositing buffer to reduce transport delay. There is no mention in Kajiya of a single buffer that is used to reduce transport delay.

Additionally, the compositing buffer is not used in Kajiya for simultaneous rendering and display of a computer image, as the single pixel buffer is in the claimed invention. Rather, rendering of the image occurs in the Tiler 200 (FIG. 4a), as previously discussed. The image is then sent into the gsprite engine 204 where the chunks are warped using the affine transform. The warped chunks are then sent through post processing and then composited and stored in one frame of the double buffered compositing buffer, then toggled to the other buffer in the compositing buffer that can be accessed for displaying the graphical information.

The single reference to a "single rasterization buffer" in the summary of the Kajiya patent is not synonymous with the single pixel frame buffer disclosed in the present application and recited in independent claim 10. The rasterization buffer disclosed in Kajiya is a group of buffers, including the double buffered pixel buffers. Kajiya does not disclose the use of a single buffer compositing buffer, a single buffer rasterization buffer, or any type of single buffer used to reduce transport delay. Nor does Kajiya describe the added complexity that would be needed to enable two separate processes to read and write to the same memory to allow simultaneous rendering and display, as previously described.

Therefore, Appellants respectfully submit that independent claim 10 presents patentable subject matter, and that the rejection of this claim should be overturned.

Rejection of the dependent claims 11 and 13 should also be overturned for at least the reasons given above with respect to the independent claim. The dependent claims, being narrower in scope, are allowable for at least the reasons for which the independent claim is allowable.

D. Rejections Under 35 U.S.C. § 103(a)

1. Requirements for Prima Facie obviousness

The Examiner has rejected all of the pending claims under § 103(a) as being *prima facie* obvious over a number of references. The Patent and Trademark Office (PTO), through the Examiner, has the burden of establishing a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1998). To satisfy this burden, the PTO must meet the criteria set out in M.P.E.P. § 706.02(j):

> [T]hree basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Moreover, the obviousness analysis must comply with the statutory scheme as explained by the Supreme Court in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966), namely, consideration must be given to: (1) the scope and content of the prior art, (2) the differences between the prior art and the claimed invention, (3) the level of ordinary skill in the pertinent art, and (4) additional evidence, which may serve as indicia of non-obviousness.

In order to combine references, the prior art must provide some reason or motivation to make the claimed compositions, *In re Dillon*, 16 U.S.P.Q.2d 1897, 1901 (Fed. Cir. 1990). As aptly stated in *In re Jones*, 21 U.S.P.Q.2d 1941, 1943-44 (Fed. Cir. 1992):

> "Before the PTO may combine the disclosure of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art... Conspicuously missing from this record is any

> *evidence*, other than the PTO's speculation (if it be called evidence) that one of ordinary skill in the...art would have been motivated to make the modifications of the prior art necessary to arrive at the claimed (invention)."

An excellent summary of how the prior art must be considered to make a case of *prima facie* obviousness is contained in *In re Ehrreich et al.*, 220 U.S.P.Q. 504, 509-511 (CCPA 1979). There the court states that a reference must not be considered in a vacuum, but against the background of the other references of record. It is stated that the question of a § 103 case is what the reference(s) would "collectively suggest" to one of ordinary skill in the art. However, the court specifically cautioned that the Examiner must consider the entirety of the disclosure made by the reference and avoid combining them indiscriminately.

In finding that the "subject matter as a whole" would not have been obvious in *Ehrreich* the court concluded:

> "Thus, we are directed to no combination of prior art references which would have rendered the claimed subject matter as a whole obvious to one of ordinary skill in the art at the time the invention was made. The PTO has not shown the existence of all the claimed limitations in the prior art or any suggestion leading to their combination in the manner claimed by applicants." (underlining added)

It is true that an obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been obvious where others would not. See KSR Int'l Co. v. Teleflex Inc., 550 U.S. __, 2007 WL 1237837, at *12 (2007). However, it has been widely recognized that virtually every invention is a combination of elements and that most, if not all, of these will be found somewhere in an examination of the prior art. This reasoning lead the court, in *Connell v. Sears, Roebuck & Co.*, 220 U.S.P.Q. 193, 199 (Fed. Cir. 1983) to state:

> "...it is common to find elements or features somewhere in the prior art. Moreover, most if not all elements perform their ordained and expected function. The test is whether the claimed invention as a whole, in light of all the teachings of the references in their entireties, would have been obvious to one of ordinary skill in the art at the time the invention was made." (underlining added)

With the above background in mind, Appellants contend that the Examiner has not met this burden with respect to the claims rejected under § 103. Particularly, Appellants submit that the PTO has failed to show that each and every element of the claimed invention is contained in the combined references, and that there was sufficient reason to modify the asserted prior art references to achieve the present invention. Appellants now turn to a discussion of the individual rejections at issue, and the references on which they are based.

2. The rejection of Claims 12 and 14 over Kajiya in view of Grigor

Rejection of the dependent claims 12 and 14 should also be overturned for at least the reasons given above with respect to independent claim 10. The dependent claims, being narrower in scope, are allowable for at least the reasons for which independent claim 10 is allowable.

3. The rejection of Claims 24, 26-29, 32 and 34-35 over Kajiya in view of Taraci

According to M.P.E.P. § 706.02(j), to render a claim *prima facie* obvious, the asserted prior art reference (or references when combined) must teach or suggest all of the claim limitations. Appellants submit that the combinations asserted by the Examiner does not teach or suggest each and every element of the rejected claims.

As Appellants have argued repeatedly, the elements of the method taught in Kajiya do not correspond to those of Appellants' invention.

As previously discussed, the Kajiya reference fails to teach or suggest the use of a single buffer for simultaneous rendering and display in a computer image generator. Independent claims 24 and 32 both include the limitation of rendering screen bins into a single pixel frame buffer to enable simultaneous rendering and display.

Additionally, both independent claims 24 and 32 include the limitation of displaying at least one rendered screen bin when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed. The Final Office Action mailed February 27, 2007 states that Kajiya does not specifically teach this limitation. (See page 8). However, the Examiner asserts that Taraci teaches the limitation that an output/display vertical frame read pointer is placed at a point in reference to an input/render vertical write pointer to create a frame rate delay of ½ a frame indicating that rendering is at least ½ completed before displaying begins. The Examiner cites Taraci, Col. 8, lines 30-45 to support her assertion.

Appellants respectfully disagree with the Examiner's characterization of Taraci. The citation to Taraci is in the background section of the patent. The background section discusses problems that occur with state of the art seamless graphics switchers (SGS) that are capable of switching between multiple analog and digital input formats and resolutions while keeping the output rate and resolution stable. (See Col. 4, line 65 to Col. 5, line 6).

Taraci discusses problems that occur in SGS caused by frame delays at various points in a video system. (Col. 8, lines 15-25). Taraci then discusses attributes of an SGS that would be desirable. The Examiner's citation states that:

> For example, a desirable SGS is one where the read and the write pointers in memory do not cross, and it does not produce an output frame made up of two different input frames. It is also desirable to provide a system wherein the output and input vertical sync pulses are locked, and the position of the output vertical frame read pointer in memory can be adjusted as compared to the position of the input vertical frame write pointer. For instance, a desirable SGS would allow the output read pointer to be placed at any point in reference to the input vertical pointer, so that for instance, frame rate delay could be adjusted (e.g. to say, half a frame). Thus, frame rate delay for an SGS could be set at, adjusted to, or programmed to change to one or more constant, predictable values as desired. (Col. 8, lines 30-45).

While it may be desirable to allow a frame rate delay for a seamless graphics switcher to be adjusted, Appellants do not believe that this citation, or anywhere in Taraci, teach or suggest the limitation of displaying at least one rendered screen bin when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed. Therefore, the combination of Kajiya and Taraci would not result in all of the limitations of independent claims 24 and 32. Rather, the combination of Kajiya and Taraci would result in a graphics generator configured to affine transform chunks, composite the chunks in a double buffered compositor buffer, and double the number of lines of resolution at the output of the buffer. Of course, the additional signal processing and buffering disclosed in Taraci would result in substantial additional delays in the transport delay. Thus, the combination of Kajiya and Taraci teaches away from the present invention, which reduces transport delay by enabling the simultaneous rendering and display in a computer image generator using a single pixel frame buffer.

For the reasons stated above, Appellants respectfully submit that independent claims 24 and 32 present patentable subject matter, and that the rejection of these claims should be overturned.

Rejection of the dependent claims 26-29 and 34-35 should also be overturned for at least the reasons given above with respect to the independent claims. The dependent claims, being narrower in scope, are allowable for at least the reasons for which the independent claims are allowable.

CONCLUSION

Appellants respectfully submit that the claims on appeal set forth in the Appendix are patentably distinct from the asserted prior art references. Particularly, none of the asserted references or combinations of references motivates, teaches, or suggests one of ordinary skill in the art within the meaning of 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a) to arrive at the presently claimed invention. Appellants contend that neither Kajiya alone nor Kajiya in combination with Taraci and/or Grigor teach each and every element of the claimed invention, and furthermore that they provide no reason to combine them.

For these reasons, Appellants respectfully request that the Board of Appeals reverse the rejection and remand the case to the Examiner for allowance.

Dated this 3rd day of December, 2007:

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VIII. CLAIMS APPENDIX

1-9 (canceled)

10. A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins;

(b) storing primitives in each screen bin the primitives touch;

(c) rendering the screen bins by row from top to bottom, into the single pixel frame buffer;

(d) displaying at least one row of screen bins rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins takes place after a selected portion of the screen bins for a current field have been rendered.

11. A method as in claim 10 further comprising the step of reducing the transport delay without allowing the display step to overlap a rendering envelope.

12. A method as in claim 10 further comprising the step of reducing the transport delay and allowing the display step to overlap a rendering envelope.

13. A method as in claim 10 further comprising the step of rendering at least one row of screen bins before the display step begins.

14. A method as in claim 10 further comprising the step of reducing the transport delay by allowing the display step to overlap a rendering envelope without allowing pixels from a previous field to be displayed.

15-23. (canceled)

24. A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins;

(b) storing primitives in each screen bin containing a portion of the primitive;

(c) rendering the screen bins, by row from top to bottom, into the single pixel frame buffer;

(d) displaying at least one rendered screen bin when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed.

25. (canceled)

26. A method as in claim 24, further comprising the step of using a hardware interlock to ensure that the rendering step does not advance ahead of the display step.

27. A method as in claim 26, further comprising the step of using a row based hardware interlock to ensure that the rendering step does not advance ahead of the display step.

28. A method as in claim 24, further comprising the step of executing the rendering and displaying steps concurrently within the same frame buffer.

29. A method as in claim 24, wherein step (d) further comprises using an independent timer to control toggling of the geometry buffer.

30. (canceled)

31. (canceled)

32. An image generator with a single pixel frame buffer enabled for simultaneous rendering and display, comprising:

(a) a geometry buffer divided into a plurality of screen bins;

(b) a plurality of primitives, stored in all of the screen bins that touch a screen region defined by the screen bin;

(c) a rendering engine, configured to render the primitives in the screen bins into the single pixel frame buffer by row and from top to bottom;

(d) a display processor, configured to display at least one rendered screen bin on a display screen before the rendering engine has completed rendering all the screen bins;.

(e) wherein the display processor begins to display the screen bins rendered when the rendering of the screen bins is at least ½ complete.

33. (canceled)

34. An image generator as in claim 32, further comprising a geometry engine configured to transform a database and the plurality of primitives used by the image generator.

35. An image generator as in claim 32, further comprising a real-time controller configured to receive real-time control information and compute transformation matrices.

36-38. (canceled)

IX. EVIDENCE APPENDIX

I. Moon, "ESIG-3000/2000 System Overview," June 3, 1991

X. RELATED PROCEEDINGS APPENDIX

(No matter presented)